WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising plural transistor element regions formed in a semiconductor layer within a same chip, and a wiring region formed by laminating plural metal wiring layers and interlayer films on the top of the transistor element regions,

wherein a dielectric constant of a specified portion of the interlayer film laminated on the transistor element regions is different from a dielectric constant of the interlayer film in areas other than the specified portion.

2. The semiconductor memory device according to claim 1, wherein the specified portion is a region on the transistor element region for composing a memory cell out of the plural transistor element regions.

3. The semiconductor memory device according to claim 2, wherein the specified portion is positioned on an N-well region for forming the transistor element.

4. The semiconductor memory device according to claim 2, wherein the specified portion is positioned on a P-well region for forming the transistor element.

5. The semiconductor memory device according to claim 2, wherein the specified portion is positioned in a layer between the highest layer for composing the transistor element and the metal wiring layer for electrically connecting with the transistor element.